SPECIFICATION

DVBS TUNER Revision:1.1

1.SCOPE

The DVBS2-6899 supports QPSK in DIRECTV and DVB-S legacy transmission (up to 45 Mbauds), plus 8PSK in DVB-S2 transmissions (up to 30 Mbauds). DVB-S2 demodulation uses robust symbols probust by the transmission to ensure efficient carrier tracking. Carrier and timing recovery loops are fully digital and tunable. Carrier-to-noise ratio (CNR) calculation and constellation display are also supported.

2.GENERAL SPECIFICATIONS

2-1. Receiving Frequency : 950~2150 MHz

2-2. RF Input Impedance : 75 OHM

2-3 RF Loop out Impedance : 75 OHM

2-4 Lo PLL Synthesizer IC : Built in PLL
(IC Bus: STB6100)

2-5 RF Input Connector : F Type (Female)

2-6 RF Loop out Connector : F Type (Female)

2-7 PLL Step Size : 1MHz

2-8 Operating Voltage .LNB Power :(TYP)
.Supply Voltage
1)Supply voltage for LNA : B1, 5V
2)Supply voltage for Tuner IC : B2, 5V
3)Supply voltage for DMIC : B3, 1.2V ; B4, 3.3V

Pin No.	Min.	Typ.	Max.
4	4.75V	5V	5.25V
5	4.75V	5V	5.25V
21	3.13V	3.3V	3.47V
10	1.18V	1.2V	1.22V

2-2. Temperature Range
Storage Temperature : -20°C ~ + 80°C
Operation Temperature : 0°C ~ + 50°C

2-3. Weight : 50g

3.TEST CONDITIONS

3-1. Test conditions : All data held under following conditions
: +25+/-2°C / Humidity : 45 ~ 65% RH

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4.ELECTRICAL SPECIFICATION OF THE RF TUNER

Test Condition	1.Supply Voltage 1-1 Supply Voltage (B1,B2) : 5V +/- 0.1V DC 1-2 Supply Voltage (B4) : 3.3V +/- 0.1V DC 1-3 Supply Voltage (B3) :1.2V +/- 0.05V DC 2.Ambient Temperature : 25°C +/- 5°C 3.Ambient Humidity : 65% +/- 10%

NO	ITEM	SPECIFICATION				CONDITION
		MIN	TYP	MAX	UNIT	
4-1	Input Level	-69		-25	dBm	
4-2	RF Input VSWR			3		
4-3	Noise Figure		6	12	dB	
4-4	Loop through specification 950MHz~2150MHz					
4-41	Output VSWR			2.5		75 OHM
4-42	Gain variation	-4		+4	dB	
4-43	Noise figure		7	10	dB	
4-44	Spurious at loop through		-70	-63	dBm	
4-45	2nd order intermodulation at -25dBm input			-35	dB	
4-46	3rd order intermodulation at -25dBm input			-50	dB	
4-47	Isolation RF out to IF test			-20	dB	
4-48	Isolation RF out to RF in			-20	dB	
4-5	3rd order Intermodulation Rejection Ratio	40			dBc	Two tone input level are -30dBm, respectively.
4-6	Local Oscillation Signal leakage at RF Input Terminal		-80	-63	dBm	950-2150MHz
4-7	Phase Noise 1KHz offset 10KHz offset 100KHz offset		 -80 -90 -95	 -70 -80 -90	 dBc/Hz dBc/Hz dBc/Hz	
4-8	I/Q Level balance		+/-1	+/-3	dB	I Relative
4-9	I/Q Phase balance		+/-3	+/-5	DEG	
4-10	Supply current B2, Operation mode B2, Power down mode B1		 195 52 16		 mA mA mA	 See register LPEN
4-11	Noise figure		9	12	dB	At ,max gain
4-12	AGC range	60	70		dB	

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5. Tuner PLL PROGRAMMING

Table 1 : Control Bit summary

Name	Size	Description
VCO [7:0]	8 bit	VCO search and VCO divide ratio
NI [7:0]	8 bit	N counter integer value
NF [9:0]	10 bit	N counter fractional value
K [1:0]	2 bit	Crystal oscillator output enabled or disabled
PSD2	1bit	VCO prescaler setting
GCT[2:0]	3 bit	Baseband VGA gain setting
G[3:0]	4 bit	Baseband programmable gain setting
F[4:0]	5 bit	Adjustable baseband LPF nominal bandwidth setting
DLB [2:0]	3 bit	DC servo loop bandwidth control
FCCK	1 bit	LPF bandwidth setting clock enabled or disabled
BEN	1 bit	Power down the bias circuitry
OSCP	1 bit	Power down the VCO
SYNP	1 bit	Power down the synthesizer
LPEN	1 bit	PLL loop enable
LD	1 bit	PLL lock detector

Table 2 : Write data definition

Register	Address	MSB	Control byte						LSB
Address	0xC0	1	1	0	0	0	0	0	0
VCO	0x01	OSCH	OCK1	OCK0	ODIV	OSM3	OSM2	OSM1	OSM0
NI	0x02	NI7	NI6	NI5	NI4	NI3	NI2	NI1	NI0
NF	0x03	NF7	NF6	NF5	NF4	NF3	NF2	NF1	NF0
K	0x04	K1	K0	1	1	1	PSD2	NF9	NF8
G	0x05	GCT2	GCT1	GCT0	1	G3	G2	G1	G0
F	0x06	1	1	0	F4	F3	F2	F1	F0
DLB	0x07	1	1	DLB2	DLB1	DLB0	1	0	0
TEST1	0x08	1	0	0	0	1	1	1	1
FCCK	0x09	0	FCCK	0	0	1	1	0	1
LPEN	0x0A	BEN	OSCP	SYNP	LPEN	1	0	1	1
TEST3	0x0B	1	1	0	1	1	1	1	0

Table 3 : Read-only data defintion

Register	Address	MSB	Control byte						LSB
Address	0xC1	1	1	0	0	0	0	0	1
LD	0x00	Reserved							LD
TESTR1	0x0C	Reserved							
TESTR2	0x0D	Reserved							

The internal PLL (with external loop filter) is a delta sigma fractional-N synthesizer. Since this is a direct conversion tuner:

* $f_{LO} = f_{RF\ in}$

The LO is divided down from the VCO:

* $f_{LO} = f_{VCO}/m$

The VCO frequency is determined by the following formula:

* $f_{VCO} = f_{XTAL} \times P \times (N_I + (N_F / 2^9))$

where f_{LO} is the LO frequency,

$f_{RF\ IN}$ is the desired channel frequency,

f_{VCO} is the VCO output frequency,

m is the LO divide ratio (either 4 or 2, see Table 4),

f_{XTAL} is the crystal frequency, which is 27 MHz,

P is the prescaler divider value (either 2 or 1 see Table 4),

N_I is the N integer counter value,

N_F is the N fractional counter value.

5.1 Register descriptions

LD **Lock detect**

7	6	5	4	3	2	1	0
Reserved							LD

Address: 0x00

Type: Read only

Description: This register can be read to determine if the PLL is locked.

[7:0] Reserved (values not applicable).

[0] LD:PLL lock.

0:PLL is not locked 1:PLL is locked

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VCO **VCO search and VCO divide ratio**

7	6	5	4	3	2	1	0
OSCH	OCK1	OCK0	ODIV	OSM3	OSM2	OSM1	OSM0

Address : 0x01

Type: Read/write

Description :

[7] **OSCH**:VCO search.[1]

0:VCO search is disabled 1 : VCO search is enabled

[6.5] **OCK**: VOC search.[12]

00 : fast search 01 : medium search

10 : slow search 11 : search clock turned off

[4] **ODIV** : LO divide ratio (m). See Table 4

Table 4 : VCO divide ratio

Input frequency (MHz)	VCO frequency (MHz)	LO dividing ratio (m)	PLL prescaler divide ratio(P)
950 to 1075	3800 to 4300	4 (ODIV = 1)	2 (PSD2 = 1)
1076 to 1325	2152 to 4300	2 (ODIV = 0)	1 (PSD2 = 0)
1326 to 2150	2652 to 4300	2 (ODIV = 0)	2 (PSD2 = 1)

0 : $F_{LO} = F_{VCO}$ / 2 (LO frequency 1076 to 2150 MHz) 1: $F_{LO} = F_{VCO}$ / 4 (LO frequency 950 to 1075 MHz)

[3] **OSM**[3:0]: VCO state machine calibratoin word set according to LO frequency.

0000 : LO frequency range = 1076 to 1199 0001 : LO frequency range = 1200 to 1299

0010 : LO frequency range = 1300 to 1369 0100 : LO frequency range = 1370 to 1469

0101 : LO frequency range = 1470 to 1529 0110 : LO frequency range = 1530 to 1649

1000 : LO frequency range = 1650 to 1799 1010 : LO frequency range = 1800 to 1949

1100 : LO frequency range = 1950 to 2150 1010 : LO frequency range = 950 to 999

1100 : LO frequency range = 1000 to 1075

1.Disable OSCH (set to 0) and turn off OCK (set to 11) after the tuner is locked.

NI **N counter integer value**

7	6	5	4	3	2	1	0
NI7	NI6	NI5	NI4	NI3	NI2	NI1	NI0

Address : 0x02

Type : Read / write

Description :NI is used in the equation $F_{VCO} = F_{XTAL} \times P \times (N_I+(N_F/2^9))$ to determine the VCO frequency, where N_I is the decimal value of NI [7:0].

NF **N counter fractional value**

7	6	5	4	3	2	1	0
NF7	NF6	NF5	NF4	NF3	NF2	NF1	NF0

Address : 0x03

Type: Read / write

Description : NF is used in the equation $F_{VCO} = F_{XTAL} \times P \times (N_I+(N_F/2^9))$ to determine the VCO frequency, where N_F is the decimal value of NF[9:0].

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K **Crystal oscillator output control**

7	6	5	4	3	2	1	0
K1	K0	1	1	1	PSD2	NF9	NF8

Address : 0x04

Type : Read / write

Description :

[7:6] **K**:crystal oscillator output control.

00 : output enabled 11 : output disabled

[5:3] **Reserved**: must always be written as 111.

[2] **PSD2** : VCO prescaler setting.

0:VCO /1,prescaler disabled (for LO frequency 1076 to 1325 MHz)

1:VCO /2,prescaler disabled (for LO frequency 950 to 1075 MHz and 1326 to 2150 MHz)

NF[9:8]:see register NF.

G **Baseband programmable gain setting**

7	6	5	4	3	2	1	0
GCT2	GCT1	GCT0	1	G3	G2	G2	G0

Address : 0x05

Type: Read / write

Description :

[7:5] **GCT[2:0]**: baseband VGA gain setting.

000 : baseband VGA gain is unmodified (for up to $1V_{P-P}$ baseband output levels).

001 : entire baseband VGA gain curve is increased 3 dB

(for $1V_{P-P}$ to $2V_{P-P}$ baseband output levels)

[4] **Reserved** : must always be written as 1.

[3:0] **G[3:0]**:baseband gain = (G-7) x 2 (dB), where G is the decimal value of G[3:0].

Valid G range is 0010 to 1110, which corresponds to baseband gain setting of -10 dB to + 14 dB.

For example, G = 0111 sets baseband gain to (7 - 7) x 2 = 0 dB.

1110 : +14 dB 1011 : +8 dB

1001 : +4 dB 0111 : 0 dB

0101 : -4 dB 0010 : -10 dB

F **LPF nominal bandwidth**

7	6	5	4	3	2	1	0
1	1	0	F4	F3	F2	F1	F0

Address : 0x06

Type: Read / write

Description :

[7:5] **Reserved** : must always be written as 110.

[4:0] **F[4:0]** : LPF nominal 3 dB BW = F + 5 (MHz), where F is the decimal value of F[4:0].

For example, F[4:0] = 0 1111 sets LPF nominal BW to 15 + 5 = 20 MHz

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DLB **DC servo loop bandwidth control**

7	6	5	4	3	2	1	0
1	1	DLB2	DLB1	DLB0	1	0	0

Address : 0x07

Type : Read / write

Description :

[7:6] **Reserved** : must always be written as 11.

[5:3] **DLB[2:0]** : DC servo loop handwidth setting

000 : DC loop BW = 80 Hz max 001 : DC loop BW = 160 Hz max

010 : DC loop BW = 320 Hz max 011 : DC loop BW = 500 Hz max

[2:0] **Reserved** : must always be written as 100.

FCCK **LPF bandwidth setting clock control**

7	6	5	4	3	2	1	0
0	FCCK	0	0	1	1	0	1

Address : 0x09

Type : Read / write

Description:

[7] **Reserved** : must always be written as 0.

[6] **FCCK** : LPF bandwidth setting clock control.[1]

0:LPF BW setting clock it turned off 1:LPF BW setting clock is enabled

[5:0] **Reserved** : must always be written as 001101.

1. To eliminate possible spurs, turn off LPF BW setting clock after the PLF BW is set (first write to the tuner to set LPF BW (FCCK = 1). Wait approximately 10 ms, then turn off the clock (FCCK = 0).)

LPEN **Power down and PLL enable**

7	6	5	4	3	2	1	0
BEN	OSCP	SYNP	LPEN	1	0	1	1

Address : 0x0A

Type : Read / write

Description :

[7] **BEN** : power down for bias circuitry.

0 : bias circuitry is powered off 1: normal operation

[6] **OSCP** : power down for VCO.[1]

0 : VCO is turned off 1: normal operation

[5] **SYNP** : power down for synthesizer.1

0 : synthesizer is turned off 1: normal operation

[4] **LPEN** : PLL loop enable.[2]

0 : PLL loop is disabled 1: PLL loop is enabled

[3:0] **Reserved** : must always be written as 1011.

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6.GENERAL SPECIFICATION OF THE FEC (STB0899)

6-1 MulitiStandard Demodulation	compatible with direct conversion tuners legacy DVB-S and DIRECTV™ DVB-S2 up to 90 Mbps channel bit rate multi-tap equalize for RF reflection removal
6-2 Maximum Symbol Rate	QPSK/LDPC/PCH : 20-30Mbps 8PSK/LDPC/BCH : 10-30Mbps DVB : 2-45Mbps
6-3 Half Nyquist Baseband Filter (Roll off factor)	0.35 for DVB and 0.2 for DSS & DVB-S2
6-4 Supported Code Rate	QPSK : 1/2,3/5,2/3,3/4,4/5,5/6,8/9,8/10 8PSK : 3/5,2/3,3/4,5/6,8/9,9/10
6-5 DiSEqC	DiSEqC™ 2.0 22KHz to 100KHz interface flexible GPIOs and interrupts
6-6 I^2C or 8-bit interface	
6-7 LINK IC	STB0899
6-8 DATAOUTPUT	Parallel or Serial Possible

6-9 Recommended Operating Condition

Pin No.	Parameter	Min.	Typ.	Max.
21	B4	3.135V	3.3V	3.465V
10	B3	1.19V	1.25V	1.31V

6-10 Current Consumption

Pin No.	Parameter	Min.	Typ.	Max.
21	B4		51mA	70mA
10	B3 1.2V DVBS		140mA	200mA
10	B3 1.2V DVBS2		890mA	1100mA

6-11 RESET

Minimum pulse duration	10us

*The /RESET pin should be held low until after both power supplies (1.2 V and 3.3V) have been brought up.

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7. ENVIRONMENTAL SPECIFICATION. Control refer to STB0899

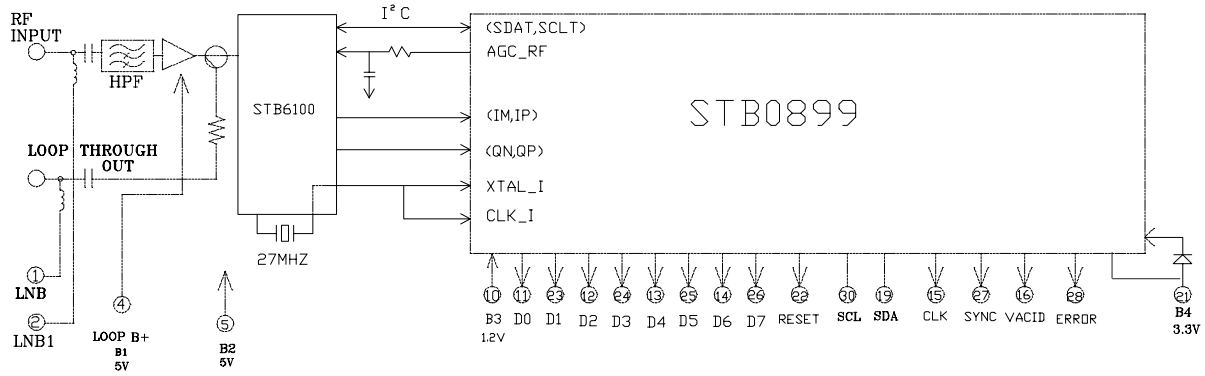
7-1 TEMPERATURE *OPERATING : 0°C TO 60°C
*STORAGE :-20°C TO 70°C

7-2 HUMIDITY *OPERATING :less than 85%
*STORAGE :less than 90%

8. ELECTRICAL SPECIFICATION OF THE CHANNEL

MODE	CODE RATE	C/N (Max.)	Unit
DVB.S	1/2	4.2	dB
	2/3	4.8	
	3/4	5.8	
	5/6	6.9	
	7/8	7.6	
DSS	2/3	4.5	
	6/7	6.7	
DVB.S2 (LDPC+BCH QPSK)	1/2	1.0	
	3/5	2.3	
	2/3	3.1	
	3/4	4.1	
	4/5	4.7	
	5/6	5.2	
	8/9	6.2	
	9/10	6.5	
DVB.S2 (LDPC+BCH 8PSK)	3/5	5.5	
	2/3	6.6	
	3/ 4	7.9	
	5/6	9.4	
	8/9	10.7	
	9/10	11.0	

Circuit block diagram



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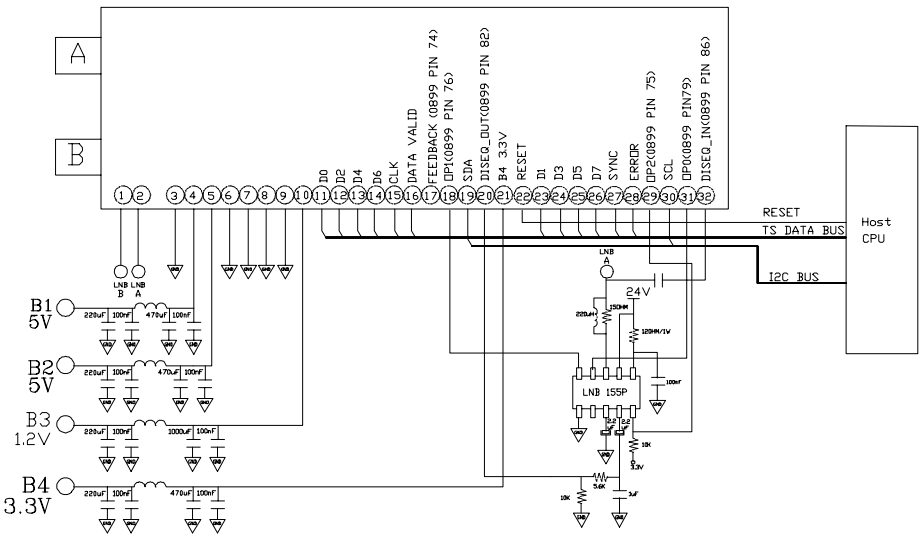
9. PIN DESCRIPTION

PIN NO	MARK	DESCRIPTION	CURRENT	RIPPLE (MAX)
1	LNB LOOP B+	POWER INPUT OF LNB LOOP B+	300mA	
2	LNB B+	POWER INPUT OF LNB B+	300mA	
4	B1 5V	5V OF RF-AMP	16mA(TYP.)	20mVp-p
5	B2 5V	5V OF TUNER ZERO IF IC	195mA	10mVp-p
10	B3 1.2V	SUPPLY VOLTAGE OF IEC IC	140mA~1100mA	10mVp-p
11	D0	DATA OUT		
12	D2	DATA OUT		
13	D4	DATA OUT		
14	D6	DATA OUT		
15	CLK	DATA CLOCK		
16	VALID	DATA VALID		
17	FEEDBACK	NC		
18	OP1	STB0899 GPIO_1		
19	SDA	I2C DATA		
20	DiseqC_out	Digital satellite equipment contorl output		
21	B4 3.3V	SUPPLY VOLTAGE OF FEC IC	51mA	10mVp-p
22	RESET	ACTIVE LOW		
23	D1	DATA OUT		
24	D3	DATA OUT		
25	D5	DATA OUT		
26	D7	DATA OUT		
27	SYNC	OUTPUT BYTE SYNC		
28	ERROR	OUTPUT ERROR SIGNAL		
30	SCL	I2C CLOCK		
31	OPO	STB0899 GPIO_0		
32	DiseqC_IN	Digital satellite equipment control input		

10. APPLICATION CIRCUIT DVBS2 TUNER



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PIN NO.	CONTENTS			
1	LNB LOOP B+	22	RESET	
2	LNB B+	23	D1	
3	GND	24	D3	
4	B1 5V	25	D5	
5	B2 5V	26	D7	
6	GND	27	SYNC	
7	GND	28	ERROR	
8	GND	29	OP2	
9	GND	30	SCL	
10	B3 1.2V	31	OP0	
11	D0	32	DISEQ_IN	
12	D2			
13	D4			
14	D6			
15	CLK			
16	VALID			
17	FEEDBACK			
18	OP1			
19	SDA			
20	DiSEQ_OUT			
21	B4 3.3V			

CUSTOM MODEL	
COMTECH MODEL	(7/7)